Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims:

1. (currently amended) An integrated circuit device that comprises:

a memory array integrated on a substrate, wherein the memory array stores data in encoded form;

a decoder integrated on said substrate, coupled to the memory array and configured to decode data retrieved from the memory array; and

a cache including a read cache and a write cache, the cache being integrated on said substrate and coupled to the memory array, wherein read and write caches are separate entities and the cache is configured to retrieve data stored in the memory array in anticipation of a request for said data and the cache and the memory array are separate entities that are coupled together.

2. (currently amended) The device of claim 1, further comprising a selection circuit integrated on the substrate and including a conflict resolution scheme for the read and write caches wherein the decoder is coupled between the memory array and the cache, and wherein the cache stores decoded data.

3. (original) The device of claim 1, wherein the cache is coupled between the memory array and the decoder, and wherein the cache stores encoded data.

4. (original) The device of claim 1, wherein the encoded form is in a set consisting of error detection codes, error correction codes, and encryption codes.

5. (original) The device of claim 1, further comprising:

a selection circuit coupled to the memory array to select a set of one or more memory cells in response to an address value; and

a sense circuit coupled to the memory array to sense data stored in the selected set of memory cells.

wherein the cache is configured to receive a read operation comprising an address value, and is further configured to provide the address value to the selection circuit if the cache does not have a copy of data stored in the corresponding set of memory cells.

6. (original) The device of claim 5, further comprising:

wherein the cache is further configured to determine a set of one or more predicted address values and to provide the set of predicted address values to the selection circuit.

7. (original) The device of claim 1, wherein the memory array comprises memory cells of a first information storage technology, and wherein the cache comprises memory cells of a second, different information storage technology.

8. (original) The device of claim 7, wherein memory cells of the first information storage technology orient magnetic fields to store information.

9. (original) The device of claim 8, wherein memory cells of the second information storage technology employ bi-stable circuits to store information.

10. (currently amended) A method of providing access to stored data, the method comprising:

receiving an address value at a cache integrated on a substrate;

retrieving encoded data associated with the address value from a memory cell array integrated on said substrate if the cache does not possess data associated with the address value;

decoding the encoded data at a decoder that is separate from the cache and integrated on the substrate; and

providing decoded data as a response to receiving said address value, wherein the cache, the decoder, and the memory cell array are separate entities that are coupled together.

11. (currently amended) The method of claim 10, further comprising wherein said retrieving comprises:

implementing a scheme to resolve conflict between a read cache and a write cache, the read and write caches being integrated on the substrate retrieving encoded data associated with a block of address values containing the received address value if the cache does not possess data associated with the received address value.

12. (currently amended) The method of claim 10 11, wherein said retrieving further comprises:

storing the retrieved encoded data in the cache.

13. (currently amended) The method of claim 10 11, wherein said retrieving further comprises:

storing decoded data in the cache.

14. (original) The method of claim 10, further comprising:

retrieving encoded data associated with a subsequent block of address values if the cache does not possess data associated with the subsequent block of address values.

15. (original) The method of claim 14, wherein the subsequent block of address values numerically immediately follows the block of address values containing the received address value.

16. (original) The method of claim 14, wherein the subsequent block of address values statistically follows the block of address values containing the received address value, and wherein the method further comprises:

maintaining for each block of address values a corresponding statistics-gathering field to predict for each block a subsequent block of address values.

17. (original) The method of claim 10, further comprising:

retrieving encoded data associated with multiple subsequent blocks of address values.

18. (original) The method of claim 17, wherein at least one of said multiple subsequent blocks immediately follows in numerical order the block of address values containing the received address value, and wherein at least one of said multiple subsequent blocks statistically follows the block of address values containing the received address value.

19. (currently amended) A digital device comprising:

a cache including a read cache and a write cache;

a memory device having a memory cell array coupled to the a separate cache, the memory cell array and cache being integrated on a same substrate; and

a selection circuit integrated on the substrate and implementing a conflict resolution scheme for the read and write caches; and

a processor coupled to the memory device and configured to operate on information stored in the memory device, wherein the cache and the memory device are separate entities that are coupled together.

20. (original) The device of claim 19, wherein the information comprises software instructions for execution by the processor, and wherein the information further comprises data to be operated on in accordance with the software instructions.

21. (previously presented) The device of claim 19, wherein the cache maintains statistics-gathering fields associated with blocks of addresses in the memory cell array of the memory device, and wherein the cache employs the fields to anticipate subsequent memory accesses by the processor.

22. (previously presented) The device of claim 19, wherein the cache comprises a memory cells of a different memory technology than the memory cell array of the memory device.